Real-time DSP-based optical OFDM transmission

Yannis Benlachtar[(1)], Rachid Bouziane[(1)], Peter Milder[(2)], Robert Koutsoyannis[(2)], Christian R. Berger[(2)], James C. Hoe[(2)], Markus Püschel[(2)], Philip M. Watts[(3)], Madeleine Glick[(4)] and Robert I. Killey[(1)]

(1) Department of Electronic and Electrical Engineering, University College London, Torrington Place, London, WC1E 7JE, UK
(2) Department of Electrical and Computer Engineering, Carnegie Mellon University, 5000 Forbes Ave., Pittsburgh, PA 15213, USA
(3) Computer Laboratory, University of Cambridge, JJ Thompson Avenue, Cambridge, CB3 0FD, UK
(4) Intel Labs Pittsburgh, 4720 Forbes Ave., Suite 410, Pittsburgh, PA 15213, USA

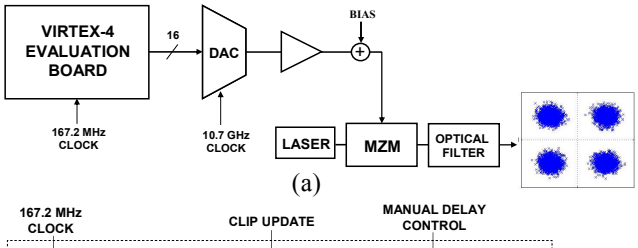
Abstract: We present the design of a field programmable gate array (FPGA) based optical orthogonal frequency division multiplexing (OFDM) transmitter operating at 21.4 GS/s and an experimental assessment of its performance in a directly-detected 8.34 Gbit/s QPSK-OFDM configuration over 1600 km of uncompensated standard fiber. We also discuss the suitability of OFDM technology for low-cost, low-power optical interconnects.

1. Introduction

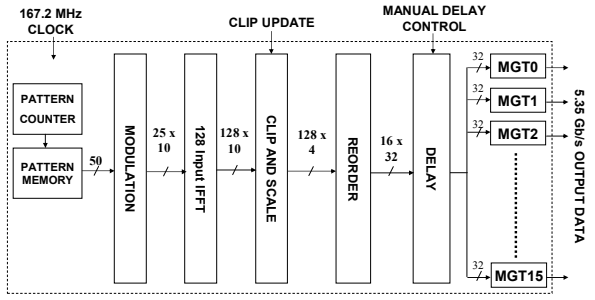
Optical orthogonal frequency division multiplexing (OFDM) is a promising technology to enable ultra-high capacity networks. Recently, real-time implementations of optical OFDM transmitters [1, 2], receivers [3] and transceivers [4] have been demonstrated using field programmable gate arrays (FPGA). In this paper we describe the design of an FPGA-based OFDM transmitter operating at 21.4 GS/s and investigate the suitability of such technology for low-cost, low-power optical interconnects.

2. Transmitter design & performance

The top level design of the optical OFDM transmitter, which consists of a DSP block, an analog section and an optical frontend, is shown in figure 1 (a). The DSP was performed on a Xilinx Virtex-4 (4VFX100) FPGA operating at a clock frequency of 167.2 MHz. The FPGA board was interfaced to a 21.4 GS/s, 4-bit resolution DAC using sixteen serial lines operating at 5.35 Gbit/s as described in [5]. The DSP block functions are illustrated in Fig. 1 (b). A 2^{15} bit sequence DeBruijn pattern and synchronization overhead were stored in a read only memory (ROM) on the FPGA and a block of N = 50 bits was read out each clock cycle and passed on to the QPSK modulator. The latter modulated the input bits to form 25 complex 10-bit QPSK codes. These were then fed to the 128-point, 10-bit IFFT core to generate single sideband OFDM signals with 1.28 oversampling. In this work, only the real output of the IFFT was utilized and sent to the clipping module to be converted into a 4-bit word compatible with the deployed DAC. The 10-bit resolution IFFT core was chosen because it offers the best trade off between system performance (signal quality) and DSP complexity [6]. It utilized a mix of radix 8 and radix 16 algorithms and was generated using the Spiral hardware generation tool to support a throughput of one transform per cycle (167.2 MHz) [7].



(a)



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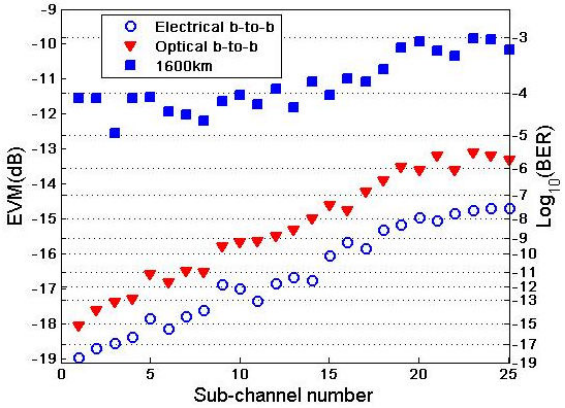

(c)

Fig. 1 (a) OFDM transmitter design (b) DSP block functions (c) EVM & BER per sub-channel [1]

First the output of the DAC was connected to a 50 GS/s real-time sampling oscilloscope to evaluate the analog quality of the OFDM signals (electrical back-to-back), using error vector magnitude (EVM). Figure 1 (c) shows the EVM and equivalent BER of each sub-channel (hollow circles). Due to the DAC frequency roll-off, the EVM increases with increasing sub-channel frequency. A similar trend can be noticed in Fig.1 (c) for the optical back-to-back configuration (using direct-detection) where a 1 dB penalty can be observed (triangles). The OFDM signal was then transmitted, by means of a recirculating loop, over 1600 km of uncompensated standard fiber with -3 dBm launch power. No cyclic prefix was implemented and dispersion equalization was performed offline at the receiver. The measured overall BER was 2×10^{-4} and EVM = -11.7 dB.

3. OFDM for optical interconnects

We studied the feasibility of using OFDM technology for low-cost, low-power optical interconnects by carrying out register-transfer-level ASIC design based on the above hardware architecture and performing simulation of the system [8]. In this work we implemented a discrete multi-tone (DMT) format where real-valued signals were obtained from a 128-point 10-bit IFFT core operating at 28 GS/s and interfaced to a 6-bit DAC. QPSK modulation was assumed with 1.28 oversampling resulting in a net output of 21.8 Gbit/s. Figure 2 (a) shows the impact of varying the FFT core resolution at the receiver assuming an 8-bit ADC and 10-bit IFFT and we found that the 14-bit FFT gives the best compromise between performance and hardware requirements. Using these parameters, we explored a range of 65nm ASIC designs with different radices, clock speeds (power consumption) and chip area and the results are shown in Fig. 2 (b). The solid lines indicate the best tradeoffs between power consumption and chip area (Pareto-optimal). The power dissipation of signal converters (DAC & ADC) and synchronization circuit were not included. The most power efficient transmitter and receiver designs were predicted to consume 7.6 and 10.7 mW/Gbit/s respectively and we expect these figures to reduce for higher order QAM and continued CMOS scaling.

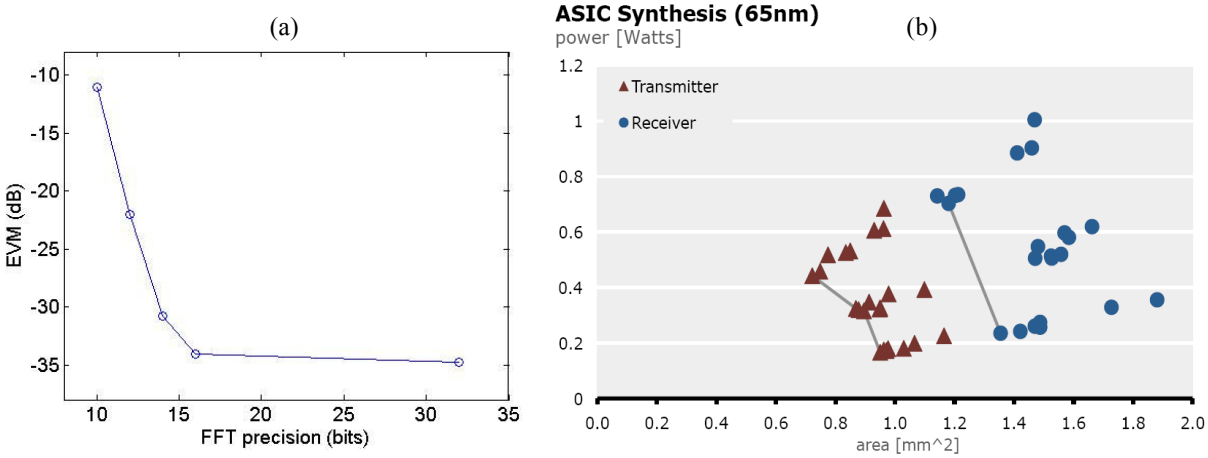

Fig. 2 (a) Received signal EVM against FFT resolution (b) Power vs. chip area for various transmitter/receiver designs [8]

4. Conclusion

We presented a 21.4 GS/s real-time FPGA-based optical OFDM transmitter that was used to generate and transmit single sideband OFDM signals over 1600 km of uncompensated standard fiber. We also carried out ASIC design studies suggesting that OFDM is a promising technology for low-cost, low-power optical interconnects.

5. References

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