Design and Simulation of 25 Gb/s Optical OFDM Transceiver ASICs

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Abstract: We select the optimum design parameters for real-time optical OFDM transceivers running at 25 Gb/s and analyze power consumption and ASIC footprint for a variety of configurations based on synthesis for a 65nm standard-cell library.

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1. Introduction

Optical orthogonal frequency division multiplexing (O-OFDM) is a potential solution for 100GbE and beyond due to its high spectral efficiency and resilience towards chromatic and polarization mode dispersion [1]. Recently many multi-gigabit real-time O-OFDM systems based on FPGA implementations have been demonstrated [2-4], since FPGAs offer a high degree of flexibility and quick implementation of proof-of-concept systems. The next step in confirming the feasibility of O-OFDM involves the design and assessment of ASIC (application-specific integrated circuit) implementations. In [5], we designed and synthesized QPSK-based 21.8 Gb/s ASIC O-OFDM transceivers, determining their area and power. In this paper, we extend this work, synthesizing and performing post-synthesis simulations of *M*-QAM O-OFDM transceivers operating at 25 Gb/s, for values of *M* ranging from 2^2 to 2^8. Based on our ASIC synthesis results, we determine the power consumption and required area of the DSP transceivers.

2. System structure

Figure 1 shows the structure of O-OFDM transceivers. The transmitter (Figure 1(a)) takes the incoming data bits and maps them to QAM symbols. A variety of *M*-QAM modulation formats are investigated, for $M=2^m$, m = 2 to 8 inclusive. The symbols are then fed to a 128-point inverse fast Fourier transform (IFFT) whose bit precision was varied from n = 6 to 20 bits (for each of the real and imaginary parts of the complex data). The output of the IFFT is clipped and scaled to be interfaced with a k-bit DAC. The resolution of the DAC, k, was varied from 3 to 12. The system used the DMT modulation format with 50 data subcarriers (causing the FFT to produce purely real data).

The receiver side is shown in Figure 1(b) where a k-bit ADC first converts the signal into the digital domain. The ADC resolution, k, was kept the same as the DAC resolution. After serial-to-parallel conversion, the OFDM signal was scaled to p bits and fed to a 128-point FFT. The FFT precision, p, was also varied from 6 to 20 bits (independent of the IFFT precision n). The output of the FFT (128 complex words) was equalized with 1-tap equalizers then fed to a symbol de-mapping block to translate from QAM symbols back to the original binary data.

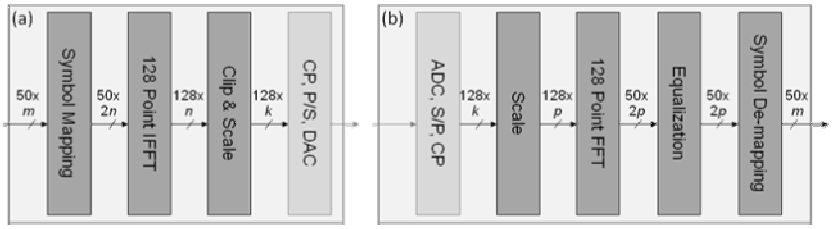

Fig. 1 (a): Transmitter design. (b): Receiver design. (CP: cyclic prefix, P/S: parallel-to-serial, S/P: serial-to-parallel.) The dark grey boxes are included in synthesized ASIC designs, while the light grey boxes are used in simulation only.

3. System characterization

First, the optimum clipping ratio was determined for different DAC resolutions. Then, the effects of IFFT/FFT bit precision were studied in an electrical back-to-back configuration. First, the IFFT bit precision was varied while using a double-precision floating FFT at the receiver. Then, the FFT bit precision was varied while using a floating

point IFFT at the transmitter. The process was repeated for all modulation formats and DAC/ADC resolutions considered above; the results for 16-QAM are plotted in Figure 2. Two regions can be identified in the plots, an (I)FFT-precision-limited region in which increasing the bit precision of the IFFT/FFT results in about 6 dB improvement in EVM and a quantization-limited region in which increasing the data converter resolution improves EVM by 5 to 6 dB per bit while increasing IFFT/FFT bit precision does not have any effect on the signal quality.

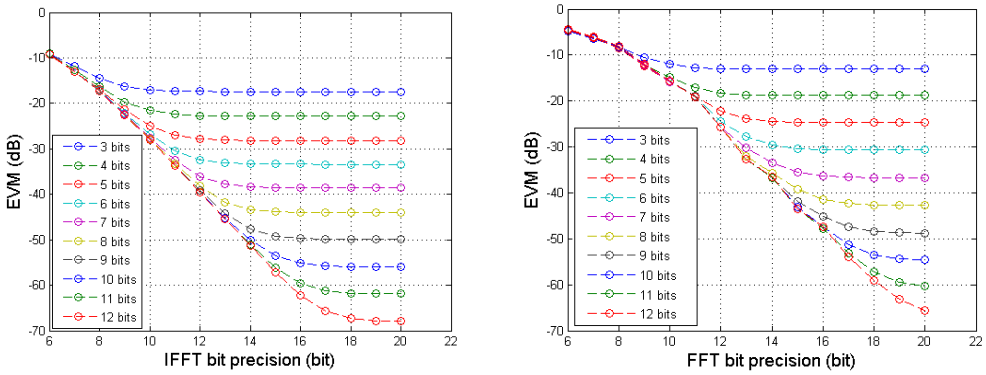

Fig. 2 Error vector magnitude (EVM) vs. IFFT bit precision (left) and FFT bit precision (right) assuming 16-QAM modulation. Each line represents a different DAC (left) or ADC (right) resolution, from 3-12 bits.

Using the system characterization results and given a target bitrate and signal quality, an optimized design can be obtained by exploring the different combinations of modulation depth, signal converter resolution, sampling speed, and arithmetic precision. The optimum designs are those that use the lowest resolution in the data converters and the minimum bit precision of the IFFT and FFT, while meeting the required EVM with a necessary margin to account for the optical components.

In this work, we considered a system running at 25Gb/s over 300 m of single-mode fiber and a bit error rate better than 10^{-3}. Following the procedure outlined above and considering the required EVM that corresponds to 10^{-3} BER for different modulation formats, we searched for optimum design parameters. The results are listed in Table 1. We then repeated the simulations using an optical link and calculated the resulting BER.

Table. 1 Different configurations for a 25Gb/s system and their requirements.

Modulation format	Min. DAC & ADC res. (bits)	Sampling rate (GS/s)	Clipping ratio (dB)	IFFT Prec. (bits)	FFT Prec. (bits)
4-QAM	4	32.0	5.5	12	14
8-QAM	4	21.4	5.5	12	14
16-QAM	5	16.0	6.5	14	15
32-QAM	5	12.8	6.5	14	15
64-QAM	6	10.7	7.5	14	16
128-QAM	6	9.1	7.5	14	16
256-QAM	7	8.0	8.5	15	16

4. ASIC design and synthesis

Given a configuration from Table 1, there are multiple hardware implementations capable of meeting the required sampling rate. Let w represent the number of samples produced or consumed each clock cycle by a given transmitter or receiver; w is thus a measure of parallelism within the transceiver. Let f be the system's clock frequency. So, $w \times f$ must equal the required sampling rate. For example, to reach 8 GS/s, a transmitter could produce 128 samples per cycle at 62.5 MHz, or 64 samples per cycle at 125 MHz, and so on. Based on this idea, a hardware generator was constructed that takes as input the parameters from Table 1 as well as values for w and f. The generator then produces synthesizable Verilog descriptions of the corresponding transmitters and receivers, using FFT and IFFT cores generated by the Spiral hardware generation tool [6].

For each configuration listed in Table 1, designs consisting of the dark grey boxes in Figure 1 were considered with w = 128, 64, 32 …, and decreasing until f reached 800 MHz. Then, each design was synthesized using Synopsys Design Compiler, targeting a 65 nm standard cell library. Figure 3 shows the area and power consumed by each synthesized design. Points closest to the lower-left corner are the most area- and power-efficient. The transmitter designs span a power range from 30 to 400 mW and an area range from 0.6 to 2 mm^2. Receivers require more area and power due to the higher precision required for the FFT and the use of complex multipliers for equalization. For any particular modulation format, the leftmost instance corresponds to the highest frequency (and

thus the lowest w), while the rightmost instance corresponds to the lowest frequency and largest w. So, as w decreases, the power requirement decreases (due to lower clock frequencies) while area increases (due to increased parallelism). Finally, the 16-QAM transceiver with the lowest power consumption was chosen for post-synthesis simulation, including optical transmission simulation.

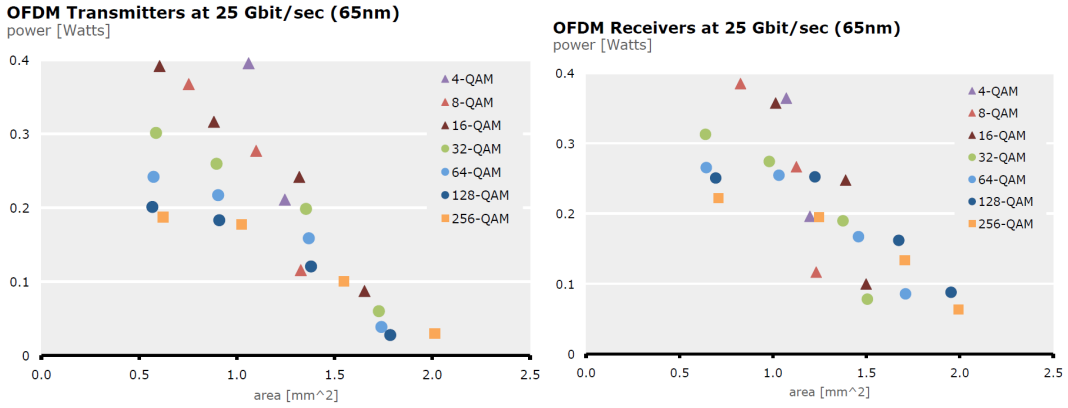

Fig. 3 Power/area results of transmitters (left) and receivers (right) for different modulation formats.

5. Post synthesis and optical link simulation

Next, the netlists produced by synthesis were tested and simulated to ensure correct functionality. The data elements from the post-synthesis designs were interfaced with Matlab models for the DAC, optical link, and ADC. The simulation modeled the signal being amplified, low-pass filtered, and fed into a linear optical modulator. Then, the model simulates optical transmission over 300m of SMF and direct detection with a photodetector. The output of the photodetector was then fed into the netlist-level simulation of the digital portion of the receiver. Simulation was performed using a length 2^{15}-1 pseudo-random bit sequence. The transmission simulation results, presented in Figure 4, show clear constellations with EVM values below -24 dB for all subcarriers which indicates that the transmission was error-free.

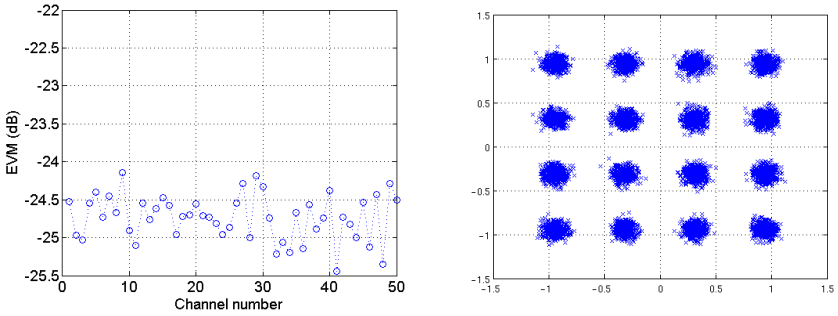

Fig. 4 Optical transmission simulation results: (Left) EVM per subcarrier and (right) the received signal constellations.

6. Conclusion

This paper considered the ASIC implementation of 25 Gb/s O-OFDM transceivers using modulation formats from 4-QAM to 256-QAM. For each modulation format, the required system parameters were determined by simulation. Then, several hardware implementations were generated for each design, and each was synthesized for 65 nm ASIC to determine its power and area requirements. Lastly, post-synthesis simulation was performed, verifying error-free transmission.

7. References

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